ESE 532 Final Report

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**1. Single ARM processor mapped design** (1 page)

1. Key parameters in the solution:
2. Performance achieved: 0.27 Mb/s (from p4)
3. Compression achieved: 4.71 Mb/s (from p4)
4. Characterization and breakdown of time spent in the major components:

**2. Ultra96 mapped design** (5 pages)

* Performance / Compression achieved
* Energy required
* Key design aspects:
  + task decomposition
  + parallelism
  + mapping to Zynq resources (with diagrams)

*Be clear where each component of the final design is performed (e.g., ARM, NEON vector, FPGA logic). Use models to explain performance.*

1. CDC - FPGA logic
2. SHA - FPGA logic (if working by tomorrow)
3. LZW and Hash Map – ARM

* Current bottleneck preventing higher performance

LZW; lowest throughput

**3. Validation** (2 pages)

· The way the code is written and mapped to the Zynq

· Testing methodology

- Use Vitis HLS to estimate the latency for each function, and get the throughput of each major component.

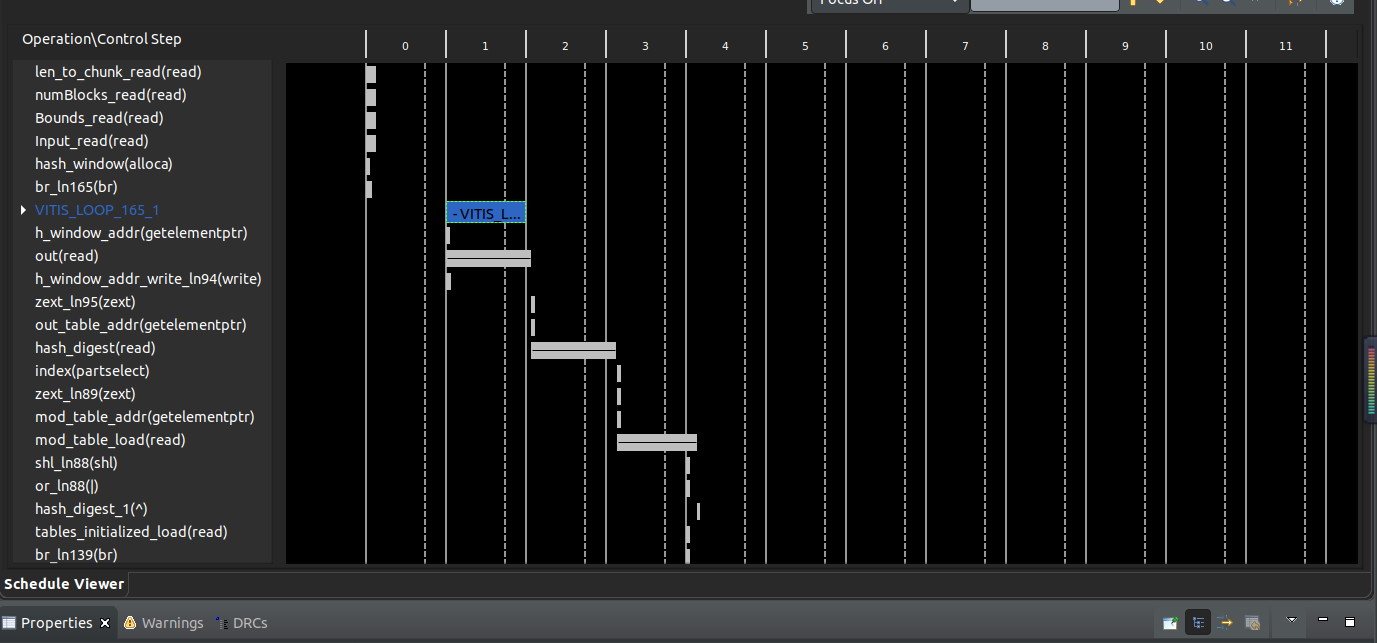
- Validate separate functions: feed different inputs to the function (LittlePrince.txt, ESE532.tar, vmlinuz.tar), check whether the output is consistent with the expectation.

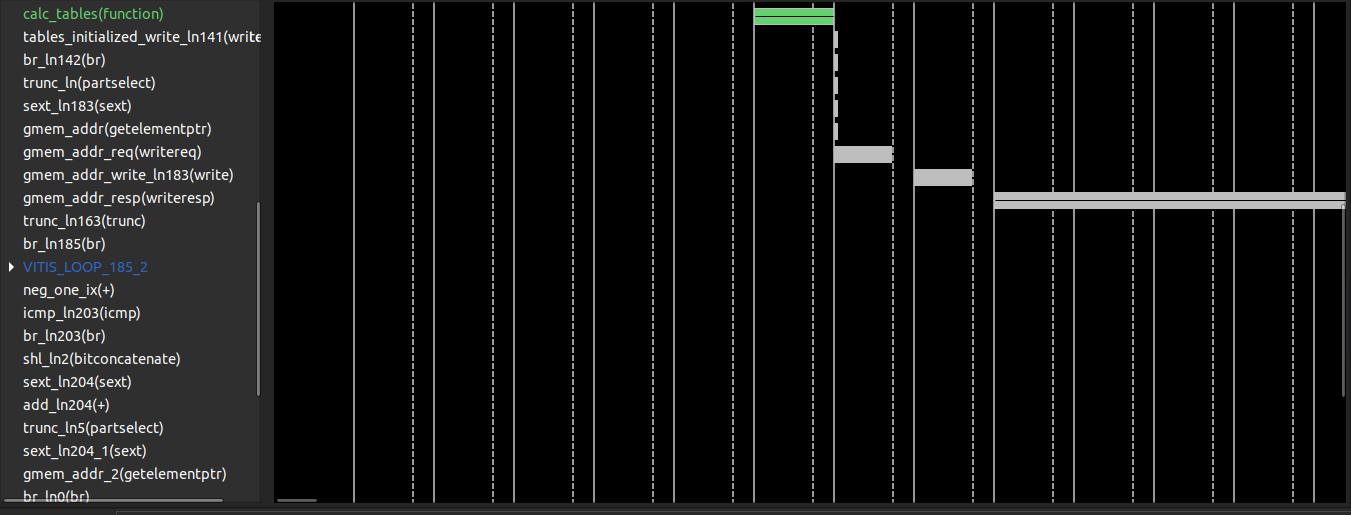
**4. Key lesson learned from the design experience** (1 page)

**5. Design space explored**

Maximized chunk size for CDC function; assign multiple compute units for the major components, splitting up the FPGA and CPU resources.

Data variables on memory: (for cdc)

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**6. Who did what**

· Sheil Sarda

· Anthony Stewart

· Shaokang Xia

**7. Academic integrity statement**

I, your-name-here, certify that I have complied with the University of Pennsylvania’s Code of Academic Integrity in completing this final exercise.